



Metuchen Capacitors, Inc.
 Toll Free 1-888-535-1535 • 732-888-9700
 1-800-679-9959/Fax
 www.metcaps.com

“We Offer Quick Solutions to Noise Pollution”

How To Select a Capacitor For Your Application

Before the proper capacitor can be selected certain electrical and mechanical parameters required by the given application must be clearly specified, the most important of which are discussed below:

For DC applications

Working Voltage (WVDC); This is specified based on the maximum potential that the selected capacitor will see in operation. It is customary to use a safety factor of 2 for most applications; that is, specify WVDC to be twice the maximum voltage the unit will see in its circuit.

Temperature Characteristic/Coefficient of Capacitance (TC); This parameter describes the manner in which capacitance value varies with operating temperature. Capacitance can change either linearly or non-linearly with temperature. In the former case the relationship would be specified as a **temperature coefficient** and expressed in parts per million of capacitance change per degree C; e.g. P090 representing a capacitance change of plus 90 parts per million (equal to 0.009%) per degree C, N750 representing a capacitance change of minus 750 parts per million (equal to -0.075%) per degree C, NP0 (negative positive zero) representing an essentially unchanged capacitance over the operating temperature range. Class I ceramic dielectrics and polypropylene and polycarbonate plastic film capacitors are examples of capacitors whose value changes linearly with temperature. The temperature dependence of units whose capacitance values vary non-linearly with temperature is specified as a **temperature characteristic**, which is defined as the percent change from the 25 degrees C value at a given temperature; e.g. X7R denotes a maximum capacitance variation of plus or minus 15% from the 25 degree value over the temperature range of -55 to +125 degrees C (typical of ceramic and tantalum oxide dielectrics), Y5V denotes a maximum capacitance variation of +22/-82% over the range of -30 to + 85 degrees. For ceramic dielectrics, it is generally true that the more negative the TC is, the smaller a capacitor's physical size will be for a given capacitance value, because, in most cases the more negative the TC is, the higher will be the dielectric constant (K).

Dissipation Factor (DF) and Q; DF is a measure of loss due to heating, expressed as a decimal. It is a unitless quantity, dependant on dielectric loss (the loss caused by the motion of electrons within the dielectric) and series resistance (ESR) contributed to by electrodes, terminations, leads, etc. From an electrical standpoint, ideally, we would like a capacitor to have a 90 degree phase angle (pure reactance). However, in the real world, the aforementioned losses cause the angle to be somewhat less than the ideal 90 degrees. Mathematically, DF is the cotangent of the actual phase angle and Q is the tangent of this angle. Hence, $Q = 1/DF$. The range of Q's available runs from about 40 for Class II dielectrics to 10,000 or more for Class I materials. For most DC applications, a DF of .025 or lower is acceptable as there is minimal current passing through the device.

Capacitance and Tolerance; For many DC applications, such as bypass and blocking, it is important to have a minimum capacitance (C_{min}) throughout the operating voltage and temperature range of the application. Since this catalog specifies nominal 25 degrees (C_{nom}) values, the minimum C_{nom} to assure that the capacitance value will not fall below C_{min} under operating conditions must be calculated.

In general

$$C_{nom} = \frac{C_{min}}{0.8 (1-T/100) (1-TN/100)}$$

where

- C_{nom} = the nominal value of the capacitor to be specified
- C_{min} = the minimum acceptable capacitance under any given conditions in the device's operating environment
- T is the negative tolerance of the device in %
e.g. T=10 for a +/-10% device, T=80 for a +10/-80% device and T=0 for a GMV device
- TN is the specified maximum negative change of capacitance over the operating temperature range, expressed in percent
e.g. TN = 15 for X7R temperature characteristic, 56 for Z5U and 82 for Y5V
- 0.8 is a compensation factor to account for voltage coefficient, ageing, etc.

Example: Circuit design requires a capacitor with C_{min} of 1000 pf. Select a capacitor with the lowest TN and widest tolerance for which C_{nom} will meet the physical size requirement of the circuit. Initially, select a device with Z5U temperature characteristic and +/-20% tolerance.

$$C_{nom} = \frac{1000}{0.8 (1-20/100)(1-56/100)} = 3551 \text{ pf}$$

Check the catalog for the next highest standard value which would be 3900 pf. If this value is available in an acceptable size and voltage rating, choose it. If not, retry with the next lowest temperature characteristic and or tolerance. Repeat until a suitable unit is found.

For AC applications

Because in AC applications appreciable current can pass through the device there is significant heating, which must be kept to a minimum. This usually means using a Class I dielectric, which has inherently lower DF but also has much lower dielectric constant (K)⁽¹⁾, which usually dictates use of a larger chip. This is not all bad as the larger chip will be capable of dissipating more of the generated heat. The desired goal should be to limit the maximum temperature of the chip to 125 degrees C. In determining this, both the maximum ambient temperature the device will operate at and the temperature rise due to current (self heating) must be considered. Hence, if a temperature rise of 20 degrees is anticipated, the maximum ambient temperature should be limited to 105 degrees. However, if the maximum ambient is going to be 85 degrees, the temperature rise due to self-heating can be as high as 40 degrees. If necessary to meet the required conditions, heat sinking or even cooling must be considered.



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The initial design approach is much the same as for DC applications, except that it is conventional to use a safety factor of 4 instead of 2. However, after calculation of C_{nom} , Power Dissipation must be evaluated:

- $I = E/Z$ Ohm's Law for AC circuits (1)
- $Z = \text{Square root } (R^2 + X_c^2)$ (2)
- $X_c = 1 / 2 \pi f c$ Definition (3)
- $R = d/2 \pi f c$ (4)
- $Z = \text{Square root } (D^2 + 1) / 2 \pi f c$ (5)
- Substituting (3) & (4) into 2
- $Z = 1 / 2 \pi f c$ Since D^2 is very small compared to 1 (6)
- $I = 2 \pi f c E$ Substituting (6) into (1) (7)
- $P = I^2 R$ (8)
- $P = 2 \pi f c (E)^2 d$ Substituting (4) & (7) into (6) (9)

Where

- P = power, watts
- E = voltage, volts
- I = current, amps
- Z = Impedance, ohms
- R = ESR, ohms
- X_c = capacitive reactance, ohms
- f = frequency, hertz
- c = capacitance, farad
- d = dissipation factor

At a minimum, power thus calculated must be correlated with the manufacturer's data to assure that the chip selected will withstand the calculated power. However, it is much better practice to use this number as a starting point and also run the specified chip at its worst anticipated operating conditions in your circuit and measure the surface temperature of the unit with a thermocouple. If this exceeds 125 degrees C, plan to use a larger chip, provide heat sinking and/or cooling or use a special high operating temperature chip. If the application requires the chip to dissipate high current or power, be sure to supply the capacitor manufacturer with all the information he needs to know this, as the chip can be designed for maximum heat dissipation. For example, as metal will conduct heat out of the chip, the design could use more layers than that for a DC or low power application. Also, you can specify larger and/or thicker termination bands than those for standard chips as they will act as heat sinks. However, in so doing it is necessary to specify a minimum separation between bands. The **theoretical** minimum separation, in mils, is equal to the required dielectric withstanding voltage (DWV) divided by 25.

Examples: For a 100 WVDC part with a 250 VDC DWV requirement the theoretical minimum distance between bands would be 250/25 or 10 mils. For a 1000WVDC part with a 1400 VDC DWV requirement the theoretical minimum separation of bands would be 1400/25 or 56 mils. In actual practice, prudent design dictates addition of 50% to 100% to the minimums thus calculated.

Important: Power Dissipation is very dependent on the specific ceramic formulation and architecture of a part. Any change in the vendor that the part is procured from, or any vendor formulation or fabrication process change, usually means that the thermal verification process must be repeated. It is a good idea to specify that no changes are to be made in the vendor's formulation or process without approval of the user. It must also be noted that charging and discharging current should be limited to 50 ma maximum to avoid component failure due to thermal shock. This is true for DC as well as AC applications because the change in voltage on charging and discharging causes current flow which can bring about enough local heating to cause failure.

Note (1)

K is a property of the dielectric material. In general, the more polar and crystalline a material is, the higher will be its K.

$$c = f (K, n, A, l/t)$$

Where c = capacitance

K = dielectric constant

n = number of layers or length of film

A = active electrode area

t = dielectric thickness

i.e. Capacitance is directly proportional to K, the number of dielectric layers in the chip or length of metallized film for plastic capacitors, and the area of the internal electrodes. It is inversely proportional to the thickness of each dielectric layer. Hence, it can be seen that to maintain a given capacitance using a lower K dielectric, one or more of the following must take place:

- (A) increase number of layers
- (B) increase active electrode area
- (C) decrease dielectric thickness

Both options (A) and (B) will increase the size of the chip. (A) will result in an increase in thickness whereas (B) will cause length and/or width to increase. Option (C) is not a good choice for a high voltage/power chip as it increases the stress on the dielectric, increasing the probability of failure.



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Typical K's and TC's for commonly used dielectrics are as follows:

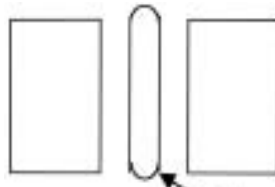
	K	TC
Polypropylene	2.5	N250 ppm/degree C
Polycarbonate	2.7	P150 ppm/degree C
Mylar polyester	3.3	+/- 3% (-25 to +85 degrees C)
High Q ceramic	6 to 16	P090 ppm/degree C
Alumina	8.4	P140 ppm/degree C
Tantalum Pentoxide	26	-10/+12% (-55 to +125 degrees C)
NP0 ceramic	30 to 90	0 +/- 30 ppm/degree C
X7R ceramic	1200 to 4000	+/- 15% (-55 to +125 degrees C)
Z5U ceramic	4000 to 8000	+22/-56% (+10 to +85 degrees C)
Y5V ceramic	8000 to 14000	+22/-82% (-30 to + 85 degrees C)

From this, it is easily seen that switching from X7R to NP0 or High Q, which is often required for high current/power applications, will result in a substantially larger chip.

ASSEMBLY NOTES

Printed Wiring Board Layout

Pad layout on the PWB should be per the EIA recommendations. However, the voltage creep must be analyzed to insure breakdown does not occur. The design goal maximum voltage stress along any dielectric interface should be less than 12.5 volts/mil, with the absolute maximum being 17.5. If the part is not coated and is surface mounted directly on the PWB, one technique to satisfy this requirement is to add a slot in the board between the pads. This places a surface discontinuity between the two voltage nodes to increase the resistance to creep.



0.050 slot between capacitor mounting pads

The 12.5 to 17.5 volts/mil maximum is also applicable from trace to trace.

Assembly Requirements

If possible, attachment to the circuit board should be achieved using solder paste and reflowing through a conveyor furnace with a controlled temperature profile to allow heating at a rate no greater than 30 degrees C per minute, to a temperature 40 to 50 degrees C above the melting point of the particular alloy in use.

When soldering the capacitor to the PWB with an iron, one with a controlled tip temperature should be used, with the temperature set to 50 degrees C above the solder's melting point. The capacitor and assembly to which it is being soldered to must be slowly elevated in temperature to the solder melting point prior to contact with the soldering iron to prevent catastrophic thermal shock to the ceramic structure.

Soldering must be done quickly, preferably with solder containing a small amount of silver as part of its formulation, to prevent leaching of the capacitor terminations. The assembly should be allowed to cool back to room temperature at its own rate.

After cooling, the assembly and circuit board surface must be thoroughly degreased to remove oils, flux, and other contaminants. This is best accomplished in a vapor degreaser. If one is not available at least two successive rinsings in a solvent(s) suggested by the flux manufacturer should do. In any event, inspect the parts for any sign of contamination.

Coatings

Voltage standoff over various environments can be improved by coating the mounted capacitor with an encapsulant or coating material. Two major factors influencing the effectiveness of a coating are its adhesion to the ceramic surface and the absence of air molecules trapped in or under the material. One material often used for this purpose is polyurethane. Various formulations of this material are available from suppliers such as Dexter-Hysol, 3M and Emerson & Cuming.

Follow the manufacturer's instructions for application and curing. It is a better to apply 2 or more thin coatings than 1 thick one.

REFERENCES

1. MIL-STD-275
2. High Voltage Design and Manufacturing Guide
 Bill Dunbar – AFWAL-TR-82-2057
 Wright Patterson Air Force Base



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